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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,687	02/12/2001	Jafar Savoj	019717-001110US	4983

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EXAMINER

CURS, NATHAN M

ART UNIT	PAPER NUMBER
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2633

DATE MAILED: 12/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/782,687

Applicant(s)

SAVOJ, JAFAR

Examiner

Nathan Curs

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-20 is/are allowed.
- 6) ☒ Claim(s) 21-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 and 7.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement (see page 12, lines 5-11). 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

2. The disclosure is objected to because of the following informalities: "signals on line 145" should be "signals on line 147" (page 6, line 19); the U.S. Patent application numbers and filing dates referred to are missing on page 12, lines 5-11; "higher low" should be "high or low" (page 14, line 2). The grammar of the sentence "The of the ERROR signal's average value is at a minimum, as is the REFERENCE signal 970" is improper (page 14, lines 16-17).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Farjad-Rad et al. (US Patent No. 5799048).

Regarding claim 21, Farjad-Rad et al. disclose a clock and data recovery apparatus comprising: a voltage controlled oscillator, configured to provide a clock signal at a clock output (fig. 3, elements 22 and CLK1); a half-rate phase detector comprising a data input, configured to receive a data input signal having a data rate and a data pattern (fig. 3, element DATA; fig. 4, element DATA; col. 1, lines 8-10 and col. 4, lines 12-20), and a clock input coupled to the clock output of the voltage controlled oscillator, configured to receive the clock signal (fig. 3, elements CLK1, CLK2, 32, 34, 40 and 42); a charge pump between the half-rate phase detector and the voltage controlled oscillator, which inputs transitioning signals and outputs a voltage level (fig. 3, element 20, and col. 1, lines 51-61), where the charge pump inherently includes a low-pass filter in order to integrate the transitioning input signals and output a voltage level. Farjad-Rad et al. also disclose that the clock signal has a frequency which is half the data rate (col. 4, lines 12-20), and the half-rate phase detector provides a first signal (fig. 3, element X1) and a second signal (fig. 3, element X2), the first signal dependent on the phase difference between the data input signal and the clock signal, and also dependent on the data pattern (col. 4, lines 12-20), the second signal dependent on the data pattern (col. 4, lines 52-61).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farjad-Rad et al. (US Patent No. 5799048) in view of Oguchi et al. (US Patent No. 4071905).

Regarding claim 22, Farjad-Rad et al. disclose a charge pump coupled between the half-rate phase detector and the voltage controlled oscillator (Fig. 3, element 20), wherein the charge pump generates an output signal by adding the second signal and the first signal and then integrating the sum to produce a voltage level (col. 1, lines 51-61). The charge pump inherently includes a low pass filter between the summing function and the voltage controlled oscillator to produce the voltage level. Farjad-Rad et al. disclose that the first and second signals are binary signals (fig. 4, element X1 and X2), but do not disclose subtracting the second signal from the first signal. Oguchi et al. disclose a binary adder/subtractor, where the output value of the adder/subtractor is the same for addition and subtraction (abstract and table 1, elements A, B and F out). It would have been obvious to one skilled in the art at the time of the invention that subtraction of the first and second binary signals, in place of the addition as disclosed by Farjad-Rad et al., could be used to produce the same result, as disclosed by Oguchi et al.

Regarding claim 23, Farjad-Rad et al. disclose that the clock signal has approximately a fifty percent duty cycle (fig. 4, element CLK1).

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farjad-Rad et al. (US Patent No. 5799048) in view of Oguchi et al. (US Patent No. 4071905), as applied to claims 22 and 23 above, and further in view of Dalmia (US Patent No. 6211741).

Regarding claim 24, Farjad-Rad et al. disclose a voltage controlled oscillator, but do not disclose that the voltage controlled oscillator comprises a ring oscillator. Dalmia discloses a phase-locked loop including a half-rate phase detector and a ring oscillator VCO (col. 2, lines 33-40 and lines 58-60; and col. 5, lines 36-42). It would have been obvious to one skilled in the

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art at the time of the invention to use the ring oscillator disclosed by Dalmia in the voltage controlled oscillator of Farjad-Rad et al. for generating complementary half-rate clock signals.

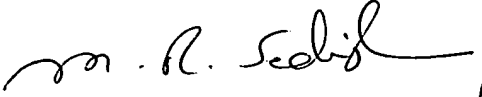
Allowable Subject Matter

8. Claims 1-20 are allowed.

Conclusion

9. Any inquiry concerning this communication from the examiner should be directed to N. Curs whose telephone number is (703) 305-0370. The examiner can normally be reached M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.


M.R. SEDIGHIAN
Patent Examiner
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